Fault Tolerant Techniques for FPGAs: A Review

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Abstract—**Field-Programmable Gate Arrays (FPGAs) have emerged as best option for digital circuit implementation over the last few decades. FPGAs have the ability to reconfigure at runtime; therefore provide opportunities to overcome issues like reliability and availability which are the serious issues in safety critical applications. This review attempts to investigate some of popular methods in fault detection and also gives an overview of partial reconfiguration technique in FPGA based systems.**

Index Terms— **FPGA, single event upsets (SEUs), SRAM, Look Up Table (LUT), Triple Modular Redundancy (TMR), Application Specific Integrated Circuits (ASIC).**

I. INTRODUCTION

Field-Programmable Gate Arrays (FPGAs) are electrically programmable silicon devices that can be used for implementing different kinds of digital systems such as DSP and network based applications. SRAM based FPGAs are used in hardware of safety critical applications, which are easily affected by radiations. FPGAs have become more vulnerable to faults like any other IC chips. SRAM based FPGAs are prone to both transient and permanent faults. Faults may occur anywhere in the device. Fault Tolerant system design involves detection of fault, diagnosis and correction of fault. But FPGA requires more area than a standard cell ASIC, has a speed performance slower than an ASIC and consumes more dynamic power. These disadvantages overcome by one major advantage which is ability to reconfigure at runtime. This review paper is structured as follows: segment 2 gives a brief overview of FPGA's architecture, segment 3 describes classification of faults and different faults Models used , segment 4 include previous related work done and segment 5 include conclusion.

II. FPGA ARCHITECTURE

FPGAs composed of a number of programmable resources which can be configured to implement any desired logical function. Fig 1 shows basic architecture of FPGA. FPGAs consist of array of programmable logic blocks, memory blocks and a multiplier blocks surrounded by programmable routing interconnects. In FPGAs, the configuration can be done at runtime; i.e. only specific parts of the FPGA can be configured without disturbing other areas from their operation. This ability is a result of partial runtime reconfiguration, Partial Reconfiguration (PR) provides a high degree of flexibility and efficiency in FPGAs.

III. FAULT TYPES, MODELS AND TOOLS

A. Fault Types:

The different types of faults that occur in FPGA-based system are categorised as follows:

- Aging faults: These are the faults occurred because of components degradation with aging.
- Manufacture Faults: stuck-at 0 or stuck at 1 type faults results from manufacturing defects.
- Single Event Upsets (SEUs) and Single Event Transients (SETs): when an energetic particle like neutron or proton collides an atom in the silicon structure, causing memory bits to alter or flips it content resulting malfunctioning of system.
- Software Faults:

B. Fault Models:

Fault models are essential for generating and evaluating test vectors. They are

- Stuck- at fault model .this may be Stuck at 0 / Stuck at 1
- Transistor stuck-on/off fault model.
- Wire open /short on interconnect.
- Delay fault model.

C. Tools :

Some of the popular tools used in FPGA systems are

- Placement and Routing Tools
- Readback
- Scrubbing
- Dynamic Partial Reconfiguration.

IV. RELATED PREVIOUS WORK DONE

In order to mitigate the effects of SEUs in FPGAs memory , many fault tolerant methods have been proposed over last few decades. These methods can be grouped into two types. (i) Based on Reconfiguration, where whenever SEU occurred, it attempt to restoring the proper values into configuration bits [5], (ii) Redundancy-based which focuses at masking the fault propagation to circuit's output [6]. Fault masking is done using Triple Module Redundancy (TMR) method, where three similar duplications of the system done in parallel and outputs of them are compared and majority voter gives the majority of three systems output as shown in Fig 2
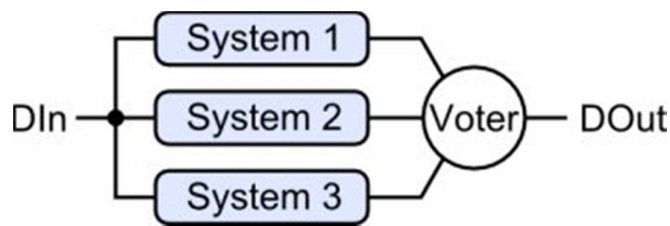

Figure 2. TMR method with Majority Voter

Memory blocks, routing blocks, and logic blocks are all vulnerable to SEUs and, thus, redundancy must be employed to overcome. The potential of the TMR method to mitigate SEUs were tested through experiments using simulation tools in earlier days [9].

Reconfiguration of memory blocks can be done using either by fine-grained or coarse-grained method. Fine-grained re-configuration is achieved by Look-Up Tables, and implementation is done with RTL Coarse-grained re-configurability is achieved by different functional units. Fine-grained method is less efficient as it consume large area overhead and causing poor *routability*. Coarse-grained method is favourite as width of path is greater than 1 bit.

Reiner Hartenstein et al[12] reviewed various architectures for coarse grain reconfigurable hardware methods which mentions architectures based on Mesh, cross bar based architectures, based on linear arrays architectures, etc.

A number of applications utilizing reconfigurable hardware and some example systems used in these applications have been discussed [14]. Reconfigurable hardware design issues which are critical to embedded system designers are also covered in the literature.

L.Sterpone et.al proposed a [18]novel technique for fault tolerant systems for SRAM based FPGAs which carry out s a set of experiments utilizing their methodology and subsequently Compares the results with existing solutions. First this technique focuses on the detection of error caused by a fault throughout the operation of system, it also identified location of such fault, quickly recovered faults to bringing the system back into the proper operation.

S. Martin et.al [19] proposed the fault tolerant design for SRAM based on FPGA using partial dynamic reconfiguration. Fig 3, shows typical block diagram of Partial dynamic reconfiguration technique. This Technique allows reconfiguration of only faulty module without affecting the operation of other module in runtime.
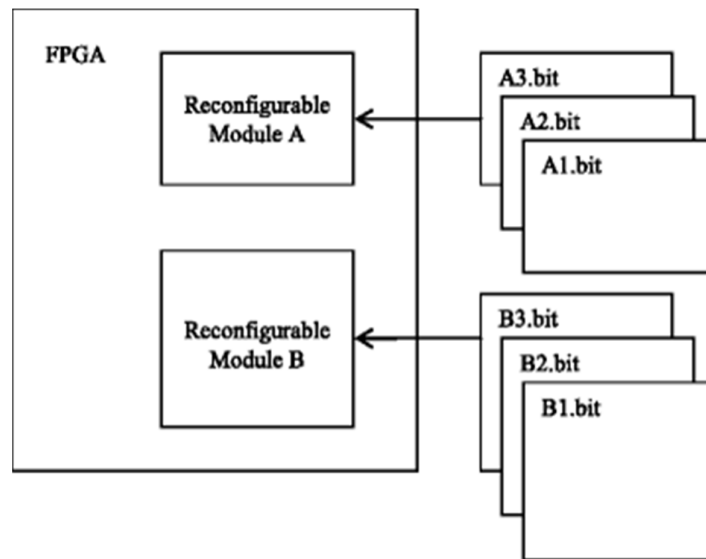

Figure 3. Partial Reconfiguration Technique

V. CONCLUSION

Many Safety critical applications demands SRAM based FPGAs because of their high-throughput capabilities and less cost. However, SRAM-based devices, are subjected to radiation affect like Single Event Upsets (SEUs) and Single Event Transients (SETs). In this review, various fault tolerant techniques for FPGA based systems has been presented along with classification of faults and popular tools. Partial reconfiguration based Fault tolerant technique is also briefly explained. Safety critical applications choose SRAM based FPGAs as primary option because of their reconfigurable ability in runtime, re-programmability, and low system development costs.

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